UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/067,805	06/28/2011	Richard Roy Grisenthwaite	SCS-550-1395	5437

73459 7590 05/01/2017

NIXON & VANDERHYE, P.C.
901 NORTH GLEBE ROAD, 11TH FLOOR
ARLINGTON, VA 22203

EXAMINER
GIROUX, GEORGE

ART UNIT	PAPER NUMBER
2182	

NOTIFICATION DATE	DELIVERY MODE
05/01/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PTOMAIL@nixonvan.com
pair_nixon@firsttofile.com

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex Parte RICHARD ROY GRISENTHWAITE

Appeal 2017-000737
Application 13/067,805
Technology Center 2100

Before DEBRA K. STEPHENS, BETH Z. SHAW, and DAVID J. CUTITTA II, *Administrative Patent Judges*.

SHAW, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant seeks our review under 35 U.S.C. § 134(a) of the Examiner's Final Rejection of claims 1–20, which represent all the pending claims. We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

INVENTION

Appellant's invention is directed to access alignment control of memory accesses in data processing systems. *See* Spec. 1, ll. 1–5.

Claim 1 is illustrative and is reproduced below:

> 1. Apparatus for processing data comprising:
> processing circuitry responsive to program instructions to perform data processing operations;
> a stack pointer register coupled to said processing circuitry and configured to store a stack pointer value indicative of an address within a memory of a stack data store;
> stack alignment checking circuitry coupled to said stack pointer register and configured to respond to a program instruction specifying a memory access to said stack data store at an address specified by said stack pointer value to detect if said stack pointer value matches a predetermined stack alignment condition;
> alignment checking control circuitry coupled to said stack alignment checking circuitry and responsive to a stack configuration parameter to selectively disable said stack alignment checking circuitry independently of further alignment checking performed upon memory accesses.

REJECTION

The Examiner rejected claims 1–8, 10–18, and 20 under 35 U.S.C. § 103(a) as being unpatentable over Circello (US 5,761,491, issued June 2, 1998) and Marshall (US 5,666,508, issued Sept. 9, 1997). Final Act. 3–8.

The Examiner rejected claims 9 and 19 under 35 U.S.C. § 103(a) as being unpatentable over Circello, Marshall, and Grisenthwaite (US 2007/0266374 A1, published Nov. 15, 2007). Final Act. 8–10.

ANALYSIS

We have reviewed Appellant's arguments in the Briefs, the Examiner's rejection, and the Examiner's response to the Appellant's arguments. We concur with Appellant's conclusion that the Examiner erred in finding that the combination of Circello and Marshall teaches "alignment

checking control circuitry coupled to said stack alignment checking circuitry and responsive to a stack configuration parameter to selectively disable said stack alignment checking circuitry independently of further alignment checking performed upon memory accesses," as recited in claim 1.

As Appellant argues, Marshall is limited to general memory accesses and does not appear to disclose stack pointers, and therefore does not teach selectively disabling stack alignment checking circuitry independently of further alignment checking performed upon memory accesses. Reply Br. 2–3. In the Final Action, the Examiner generally refers to Marshall's Abstract as teaching this element. Final Act. 4. In the Answer, the Examiner points to various teachings of Circello and refers generally to Marshall's ability to selectively disable alignment checking. Ans. 9–11. First, we agree with Appellant that the Examiner has not identified a teaching in Marshall or Circello where the selective disabling is done *independently* of further alignment checking performed on memory accesses.

Moreover, we agree with Appellant (App. Br. 9–12; Reply Br. 3–6) that the Examiner has not sufficiently explained why one of skill in the art would combine Marshall's general alignment circuitry with Circello to form the claimed alignment control circuitry that is coupled to stack alignment checking circuitry, where the alignment control circuitry is responsive to a stack configuration parameter, to selectively disable the stack alignment checking circuitry, where the selective disabling is done independently of further alignment checking performed on memory accesses.

Thus, we are persuaded by Appellant that the Examiner has not shown Circello and Marshall, taken alone or in proper combination, teaches or suggests "alignment checking control circuitry coupled to said stack

alignment checking circuitry and responsive to a stack configuration parameter to selectively disable said stack alignment checking circuitry independently of further alignment checking performed upon memory accesses," as recited in independent claim 1, and as similarly recited in independent claim 10.

Accordingly, we do not sustain the Examiner's rejection of claims 1–20.

DECISION

The decision of the Examiner to reject claims 1–20 under 35 U.S.C. § 103 is reversed.

REVERSED